The Impact of Substrate Bias on Proton Damage in 130 nm CMOS Technology

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Abstract— **The effects of proton irradiation on the *dc* and *ac* properties of 130 nm Si CMOS technology are investigated. The impact of substrate bias is reported for the first time. Two different irradiation substrate conditions were used, yielding different results. A comparison is drawn between the present work and a previously reported 180 nm CMOS technology node.**

I. Introduction

It is well known that the tolerance to ionizing radiation generally improves with CMOS technology scaling, due to the natural thinning of the gate oxide and shallow trench isolation. Circuit designers are increasingly taking advantage of the effects of both static and dynamic body (substrate) biasing to improve circuit performance (analog circuits) and reduce power dissipation (digital circuits) [1]-[3]. A reverse body bias is known to increase the threshold voltage and reduce the off-state leakage current, for instance, which is of great interest from a radiation perspective in many space-borne circuits.

This work reports for the first time the results of proton radiation on 130 nm Si CMOS technology (having an effective minimum gate length of 0.12μm) for two different irradiation substrate bias conditions. The nFETs investigated are part of a fully-integrated, third generation, 200 GHz silicon-germanium (SiGe) heterojunction bipolar (HBT) BiCMOS technology (IBM SiGe 8HP) [4]. Two types of Si CMOS devices are available in this technology 1.2V and 2.5V, with minimum channel lengths of 0.12 μm and 0.24 μm, respectively. The technology was not intentionally radiation-hardened in any way. The effects of 63 MeV proton radiation are reported here on the *dc* and *ac* performance of the 130 nm nFETs. We also compare the proton radiation tolerance observed on this 130 nm CMOS node (IBM SiGe 8HP) with those previously reported for a 180 nm CMOS node (IBM SiGe 7HP).

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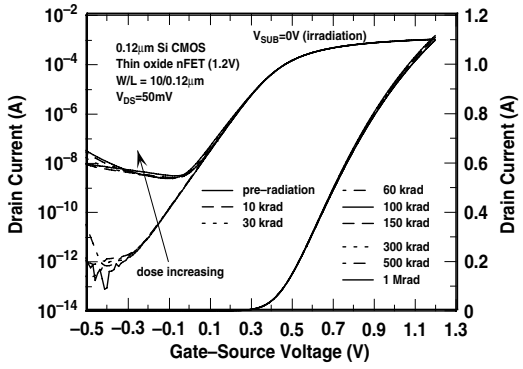

Fig. 1. Transfer characteristics for an irradiation substrate bias of 0V as a function of equivalent dose.

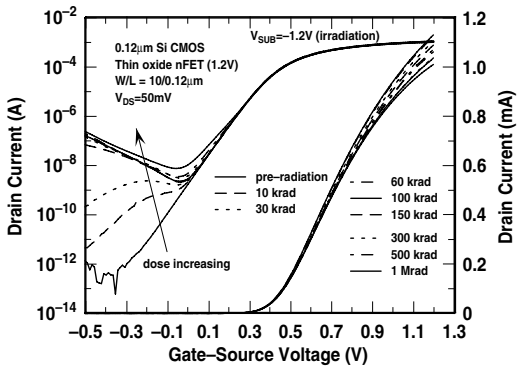

Fig. 2. Transfer characteristics for an irradiation substrate bias of -1.2V as a function of equivalent dose.

II. Experiment

Si nFETs with a channel width of 10.0 μm and lengths ranging from 1.6 to 0.12 μm were used for the *dc* investigation. The transistors were designed using conventional high-speed layouts, and do not, for instance, use annular (enclosed) layouts for reducing radiation damage. The *ac* measurements were made on multi-fingered (32 fingers) devices with a W/L of 2.0/0.12 μm per finger. The 63.3MeV proton irradiation was performed at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering foils) located several meters upstream of the target establish a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 20 nA to 80 nA allow testing with equivalent gamma doses from 10 krad to 1 Mrad. The dosimetry system was previously described [5] [6], and is accurate to about 10%.

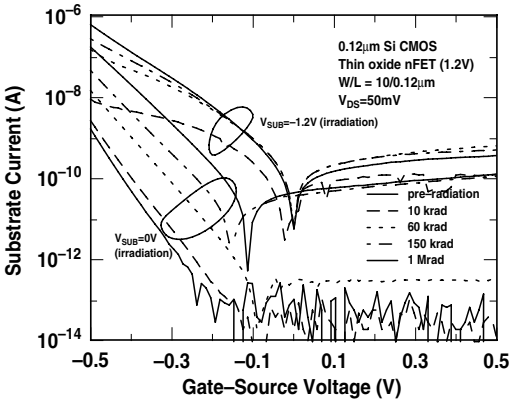

Fig. 3. Substrate current for both irradiation substrate biases as a function of equivalent dose.

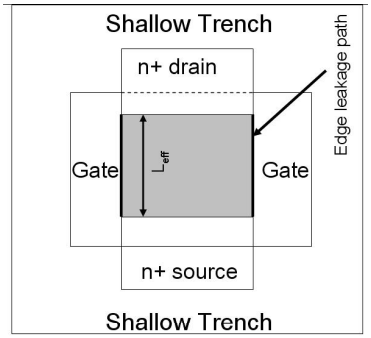

Fig. 4. A schematic top view of the STI edge leakage path.

The Si nFET *dc* test structures were irradiated at equivalent gamma doses ranging from 10 krad to 1 Mrad (proton fluences from 7.4x10^{10} to 7.4x10^{12}) under two different bias conditions. Under the first condition, the source, drain, and substrate terminals were grounded, and V_{DD} (1.2V) was applied to the gate terminal (the conventional worst case bias condition for FETs). For the second bias condition, the source and drain terminals were grounded, V_{DD} (1.2V) was applied to the gate terminal, and negative V_{DD} (-1.2V) was applied to the substrate terminal. The *ac* test structures and circuits were irradiated with all terminals floating at a dose of 1 Mrad. Wirebonding of *ac* test structures and circuits is not compatible with robust broadband measurements, and hence on-wafer probing of S-parameters was used to characterize the high-frequency performance. The samples were measured at room temperature with an Agilent 4155 Semiconductor Parameter Analyzer (*dc*) and an Agilent 8510C Vector Network Analyzer (*ac*).

III. Results and Discussion

Figures 1 and 2 depict the transfer characteristics for Si nFETs with W/L=10.0/0.12 μm with 0V and -1.2V substrate irradiation bias conditions, respectively. The substrate was grounded during measurement for both irradiation bias conditions. For the 0V irradiation substrate bias, the subthreshold leakage is essentially constant ($\sim$ 1 pA) for doses up to 60 krad and then appears to saturate at

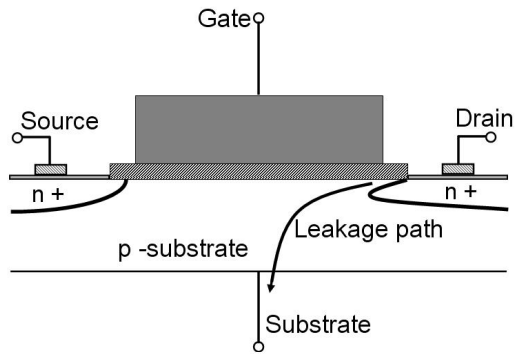

Fig. 5. A schematic view of the GIDL leakage path.

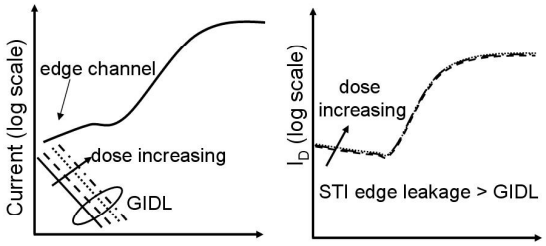

Fig. 6. Leakage current components for 0V irradiation substrate bias.

approximately 10 nA for doses from 100 krad to 1 Mrad. Observe that there is significantly more subthreshold leakage for the -1.2V irradiation substrate bias condition. The leakage occurs at doses as low as 10 krad. A similar apparent leakage saturation occurs slightly above 10 nA for doses from 60 krad to 1 Mrad. It appears that there are two fundamentally different leakage mechanisms at work for the two irradiation substrate bias conditions. In both cases, however, the off-state leakage is in the 1.0 nA/μm range, which is acceptable for many circuits, without using layout techniques or process modifications for hardening.

An examination of the substrate current versus gate-source voltage for both substrate bias conditions (see Figure 3), as well as the transfer characteristics, allows for better understanding of the leakage mechanisms in play. We believe that in both substrate bias cases the subthreshold leakage is due to a combination of two radiation induced leakage mechanisms. One cause of subthreshold leakage is the presence of radiation-induced charge physically located in the region where the gate extends beyond the shallow trench isolation (STI) edge (see Figure 4). At sufficiently high dose, a parasitic leakage path forms between the source and drain, producing a shunt leakage path [7]. A classic signature of STI edge leakage is a positive sloping drain current for gate voltage (V_G) < 0. The other cause of subthreshold leakage appears to be radiation-induced tunneling (band-to-band and/or trap-assisted) in the gate-to-drain overlap region, as evidenced by a negative sloping drain current for $V_G < 0$. This leakage mechanism is generally known as Gate-Induced-Drain-Leakage (GIDL) [8]-[9]. In GIDL, the junction field increases with decreasing gate bias, causing minority carriers under the gate to be swept into the substrate (see Figure 5), resulting in increased leakage current.

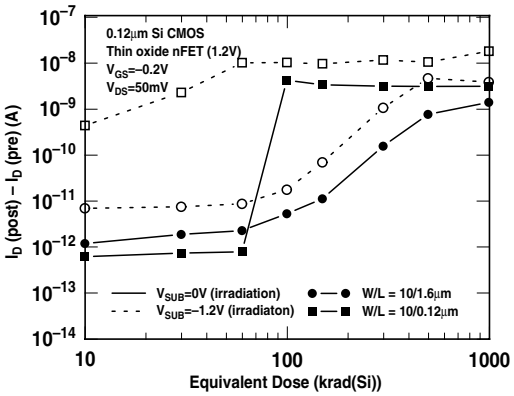

Fig. 7. Change in sub-threshold leakage as a function of equivalent dose.

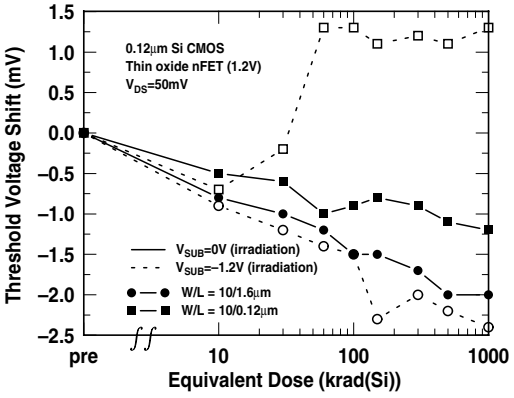

Fig. 8. Threshold voltage shift as a function of equivalent dose.

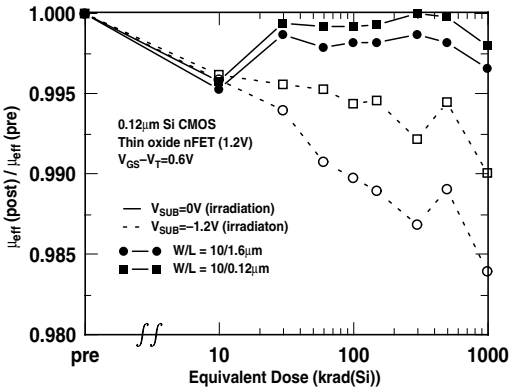

Fig. 9. Effective mobility degradation as a function of equivalent dose.

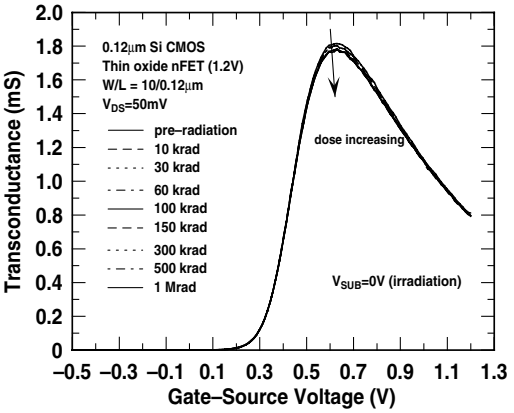

Fig. 10. Transconductance versus gate-source voltage for an irradiation substrate bias of 0V.

For the 0V substrate bias case, Figure 3 indicates a strong GIDL component that increases with increasing dose. However, the transfer characteristic (Figure 1) does not show the expected strong negative slope due to GIDL. We believe the transfer characteristic shows a "weak" negative slope because the STI edge leakage at high dose (> 60 krad) is larger than GIDL (see Figure 6). In the -1.2V substrate bias case, Figure 2 indicates the classic signature of STI edge leakage for doses of 10 and 30 krad. Above 30 krad, it appears there is a very strong GIDL component. This is corroborated by Figure 3. It seems that the GIDL component is stronger than the STI edge leakage component for the -1.2V substrate bias condition. Figure 3 indicates that GIDL saturates at high dose for the -1.2V substrate bias condition, but increases with dose for the 0V case. The GIDL component is larger for the negative bias substrate condition, presumably due in part to the higher field inducing more traps (damage) in the drain-substrate junction under irradiation. The GIDL observed in this work is clearly radiation triggered and is also dependent on the body bias during exposure; thus, it is of potential concern from a hardness assurance perspective. 2-D simulations will be required to determine the exact leakage mechanisms. As mentioned above, there is clearly more radiation induced damage for the -1.2V irradiation substrate bias. Similar stress-induced degradation has been reported for this negative substrate bias [10].

Figure 7 shows the change in net subthreshold leakage post-radiation for devices of different channel lengths (1.6 and 0.12 μm) at both substrate bias conditions. The difference in radiation-induced leakage due to substrate irradiation bias is again manifested here. In addition, we also see that the shorter channel device suffers more radiation damage than the longer channel device. This effect has previously been reported for 180 nm nFETs [11]. The threshold voltage shift ($\Delta V_T = V_{T_{post}} - V_{T_{pre}}$) was extracted for the same devices and is shown in Figure 8. There is very little change in threshold voltage up to 1 Mrad, as expected. The longer channel (L=1.6 μm) device exhibits a decrease in V_T with radiation for both substrate irradiation bias conditions, whereas the shorter channel (L=0.12μm) device demonstrates a V_T decrease only for the 0V substrate bias. Interestingly, the V_T increases after a dose of 30 krad for the short channel, negative irradiation substrate bias condition. This increase in V_T post-radiation has been reported previously for short channel devices with terminals floating during irradiation [11].

The pre- and post-radiation effective mobility (μ_{eff}) was

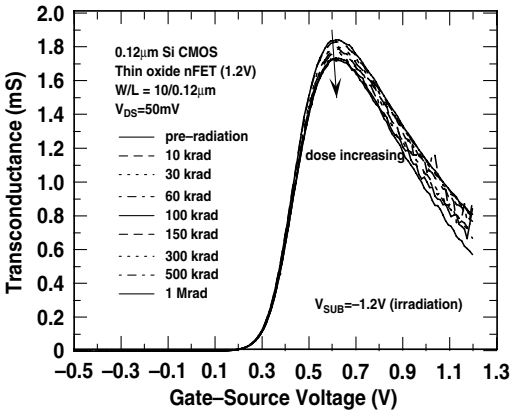

Fig. 11. Transconductance versus gate-source voltage for an irradiation substrate bias of -1.2V.

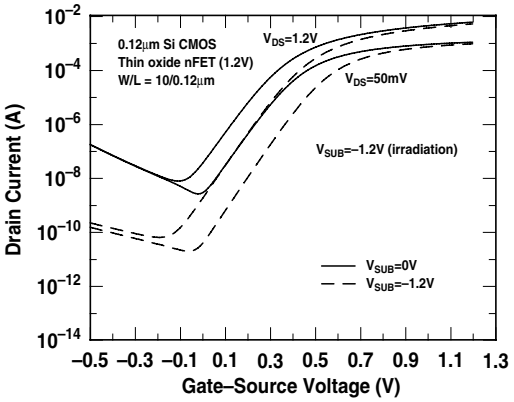

Fig. 12. Transfer characteristics after 1 Mrad equivalent dose for substrate biases of 0 and -1.2V.

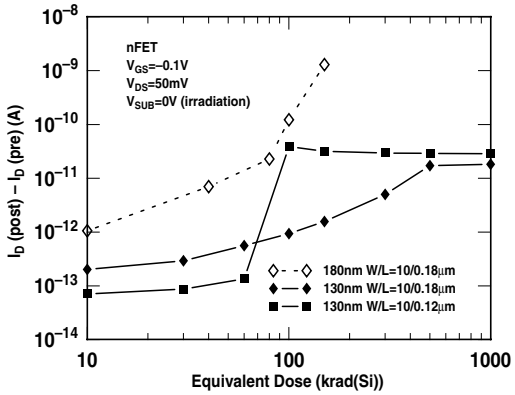

Fig. 13. Change in sub-threshold leakage for 130 and 180 nm technology nodes.

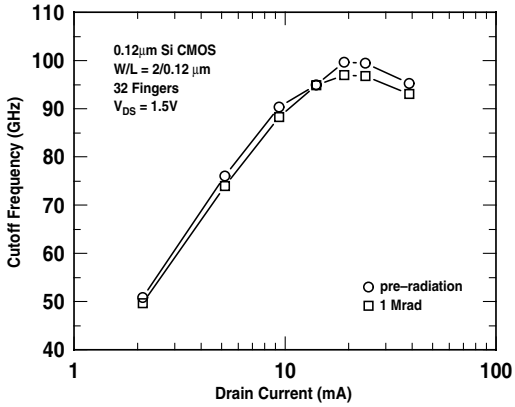

Fig. 14. Cutoff frequency as a function of drain current pre- and post-radiation.

extracted as a function of gate overdrive (V_G-V_T) using a technique capable of taking into account the bias dependence of the source-drain resistance (R_{SD}) in lightly-doped-drain (LDD) CMOS devices [12]. Figure 9 illustrates the μ_{eff} degradation as a function of equivalent dose. There is essentially no change in mobility with proton radiation for either channel length or substrate bias condition.

From the linear transfer characteristics (Figures 1,2), we see there is very little degradation in the drain current (I_D) for the strong inversion region of operation for the 0V substrate bias condition. This is not the case, however, for negative substrate bias irradiation. Here we see significant degradation in the strong inversion region. As expected, this is also apparent in the transconductance (g_m), as seen in Figures 10 and 11. Since there is very little change in both V_T and μ_{eff} post-radiation, the g_m degradation is believed to be due to an increase in R_{SD} and is consistent with enhanced damage in the gate-to-drain overlap region (i.e., the LDD) in the GIDL leakage path.

It has been previously reported that negative substrate bias during measurement can suppress the radiation-induced STI leakage. In that work, the substrate was grounded during irradiation [7]. The present work examines the effects of negative substrate bias during operation for devices irradiated with the -1.2V substrate bias condition. Figure 12 shows the I_DV_{GS} curve for a measurement substrate potential of both 0V and -1.2V, at two values of drain voltage, after 1 Mrad total dose. It is evident that a negative operational substrate bias is very effective in reducing the radiation-induced leakage, despite the enhanced damage, compared with the 0V operational substrate bias. Note that these measurements were made approximately four months after the 1 Mrad irradiation. The subthreshold leakage was essentially unchanged from that measured in-situ after 1 Mrad.

Finally, we compare the proton tolerance of this work with a previously reported 180 nm CMOS technology node [13]. The change in subthreshold leakage is shown for the 180 nm and 130 nm nFETs in Figure 13. The scaled CMOS exhibits improved radiation tolerance over the previous generation. This off-state leakage result is somewhat surprising, in fact, since the STI thickness of the 130 nm CMOS is actually slightly thicker than that for the 180 nm process. This is presumably due to the subtleties associated with the STI-to-channel physical shape at the channel edge.

The scattering parameters (S-parameters) were also measured for a thin oxide nFET with W/L = 32 gate fingers. Open and short structures were used to deembed the data in

order to calculate the small-signal current gain (h_{21}). The cutoff frequency (f_T) was determined from the magnitude of h_{21} by extrapolating a -20 dB/decade slope across a wide frequency range. The pre- and post-proton radiation f_T-I_D characteristics are depicted in Figure 14. There is an apparent very slight degradation in f_T post-radiation ($\sim 3\%$), but this is well within the error associated the measurement, and judged to be negligible.

IV. Summary

We find that grounded versus negative substrate bias during radiation produces different dominant damage mechanisms in 130 nm CMOS, and is investigated here for the first time.

V. Acknowledgement

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References

[1] X. Lui *et al.*, *IEEE ISCAS*, vol. 4 pp. 9-12, 2000.
[2] L.T. Clark *et al.*, *IEEE Trans. VLSI Systems*, vol. 12, pp. 947-956, 2004.
[3] S. Terry *et al.*, *Proc. IEEE Int. SOI Conf.*, pp. 80-82, 2002.
[4] B.A. Orner *et al.*, *Proc. IEEE BCTM*, pp. 203-206, 2003.
[5] K.M. Murray *et al.*, *Nucl. Inst. Meth.*, vol. A281, p. 616, 1989.
[6] P.W. Marshall *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1958-1965, 1994.
[7] G. Niu *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 1841-1847, 1999.
[8] T. Chan *et al.*, *Tech. Dig. IEEE IEDM*, pp. 721-724, 1987.
[9] S.A. Parke *et al.*, *IEEE Trans. Elec. Dev.*, vol. 39, pp. 1694-1703, 1992.
[10] N.R. Mohapatra *et al.*, *Proc. IEEE IPFA*, pp. 27-30, 2002.
[11] E. Simoen, *et al.*, *IEEE RADECS Conf.*, pp. 69-76, 2001.
[12] G. Niu *et al.*, *IEEE Trans. Elec. Dev.*, vol. 46, pp. 1912-1914, 1999.
[13] Y. Li *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 1834-1838, 2003.